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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,239	03/01/2002	Atul V. Ghia	X-1061 US	6539

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/090,239	Applicant(s) GHIA ET AL.	
	Examiner Anh Q. Tran	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9,16,17,19-22,24,25,29,31-33,35,36,40,42-47,57,58 and 60* is/are rejected.

7)☒ Claim(s) *7,10-15,18,23,26-28,30,34,37-39,41,48-56 and 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4 & 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Aung et al (Pub. No.: US 2001/0033188 A1).

Claim 1, Aung shows a programmable logic device (Fig. 10) comprising:

Programmable input/output circuitry (inherent element in a PLD);

Programmable core logic (80) coupled to the input/output circuitry;

A multi-gigabit transceiver (340, 60) coupled to the programmable core logic;

A first pair of clock pads (the pads connected to 42); and

A dedicated routing structure (1) directly connecting the first pair of clock pads and the multi-gigabit transceiver.

Claim 2, Aung shows a differential buffer (42a) coupled to the first pair of clock pads; and a first clock trace providing a direct connection between the differential buffer and the multi-gigabit transceiver.

Claim 3, Aung shows a second pair of clock pads (pads connected to 42b); and

A second dedicated routing structure (1 output from PLL 100b) directly connecting the second pair of clock pads and the multi-gigabit transceiver.

Claim 4, Aung shows a second differential buffer (42b) coupled to the second pair of clock pads; and

A second clock trace (1 output from PLL 100b) providing a direct connection between the second differential buffer and the multi-gigabit transceiver.

Claim 5, Aung shows a first multiplexer (360a, 540a) coupled to the first and second clock traces, the first multiplexer being configured to selectively route a clock signal on either the first or second clock trace in response to a select signal (inherent limitation).

Claim 6, Aung shows a programmable connection (522) between the programmable core logic and the first multiplexer, wherein the programmable core logic provides the select signal to the first multiplexer (it can also be true for other PLCs, col. 11, lines 7-13).

Claim 8, Aung shows the multi-gigabit transceiver further comprises a phase locked loop configured to receive the clock signal selected by the first multiplexer (150a).

Claim 9, Aung shows the multi-gigabit transceiver further comprises a serializer (340a, 60a) configured to operate in response to a serializing clock signal (output from 518a) generated by the phase locked loop in response to the clock signal selected by the first multiplexer.

Claim 16, Aung shows the multi-gigabit transceiver comprises a physical media access sublayer and a physical coding sublayer.

Claim 17, Aung shows means (540a) for routing a clock signal on the dedicated routing structure to a phase locked loop (150a) in the PMA as a PMA reference clock signal. Claim 19, Aung shows the first pair of clock pads is located near the center of an edge of the programmable logic device.

The limitations described above are applicable to the method claims 20-22, 24-25, & 29.

Aung shows a clock generation circuit (100a) coupled to the first pair of clock pads, furthermore, the rest of the limitations of claims 31-33, 35-36, 40, 42-47, 57-58, and 60 are described above.

Allowable Subject Matter

3. Claims 7, 10-15, 18, 23, 26-28, 30, 34, 37-39, 41, 48-56, and 59 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

-a second logic gate having input terminals coupled to received clock signal on the second clock trace and the inverse of the select signal, and an output terminal coupled to the second transmission gate.

-a general-purpose clock routing path coupling the down-level shifter to the multi-gigabit transceiver.

-a down-level shifter.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chan et al (Pub. No.: US 2003/0039168 A1) discloses a programmable logic device having serializer/deserializer circuit and input/output circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
June 10, 2003